

Docket No. 216692US2/smc

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Takashi YAMADA, et al.

SERIAL NO: 09/995,594

GAU: 2812

FILED: November 29, 2001

EXAMINER:

FOR: SEMICONDUCTOR CHIP HAVING MULTIPLE FUNCTIONAL BLOCKS INTEGRATED IN A SINGLE CHIP AND METHOD FOR FABRICATING THE SAME

INFORMATION DISCLOSURE/RELATED CASE STATEMENT UNDER 37 CFR 1.97

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Applicant(s) wish to disclose the following information.

REFERENCES

- ☒ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

- ☐ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

- ☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

- ☒ Please charge any additional fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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SERIAL NO: 09/995,594

Group Art Unit: 2812

STATEMENT OF RELEVANCY

Reference AM (JP 10-303385) on Form 1449:

This reference shows a similar SOI device which contains a bulk region for DRAM cell.

Reference AN (JP 8-316431) on Form 1449:

This reference shows a similar SOI device which contains a bulk region.

Reference AO (JP 7-106434) on Form 1449:

This reference shows a similar SOI device which contains a bulk region for DRAM cell.

Reference AP (JP 11-238860) on Form 1449:

This reference shows a similar SOI device which contains a bulk region for DRAM cell.

Reference AQ (JP 2000-91534) on Form 1449:

This reference shows a similar SOI device which contains a bulk region for DRAM.

Reference AR (JP 2000-243944) on Form 1449:

This reference shows a similar SOI structure which contains a bulk region.

Reference AS (JP 8-17694) on Form 1449:

This reference shows a similar SOI device which contains a bulk region.

Reference AT (JP 11-17001) on Form 1449:

This reference shows a similar SOI structure which contains a bulk region.

Reference AU (2000-269460) on Form 1449:

This reference shows a similar DRAM cell in which a transfer transistor is fabricated over a trench capacitor by using an epitaxial growth technique.

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STATEMENT OF RELEVANCY

Reference AV (JP 2001-196556) on Form 1449:

This reference shows a similar DRAM cell in which a transfer transistor is fabricated over a trench capacitor by using an epitaxial growth technique.

Reference AW on Form 1449:

This reference shows a similar SOI based embedded DRAM.

Reference AX on Form 1449:

This reference shows a similar DRAM cell in which a transfer transistor is fabricated over a trench capacitor by using an epitaxial growth technique.